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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/059,644	04/13/98	PAN	P MI22-898

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EXAMINER	
TRINH, M	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 12/19/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/059,644	PAN, PAI-HUNG	
	Examiner	Art Unit	
	Michael M. Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41 and 43-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41 and 43-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

*** Amendment filed September 28, 2000 has been entered as paper number 16/C. Claims 41,43-52 are pending. Claims 1-40,42 were canceled. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

*** In the Amendment filed September 28, 2000 (pp. 5), Applicant requested that "In claim 52, at line 15 of the claim, insert --laterally adjacent to and-- before 'covering.'". However, that "covering" is not located at line 15, but located at line 17 of claim 15 in our record. Accordingly, the phrase --laterally adjacent to and-- is inserted at line 17 of claim 15, before "covering all of". Clarification is respectfully requested in response to this office letter.

Claim Rejections - 35 USC § 112

1. Claims 43-44,47-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

** Re Claim 43, line 1; Claim 44, line 3, line 6: the terms "the gate" lacks proper antecedent basis, and should be -- the gate electrode --.

** Re Claim 47, line 1; Claim 48, line 3, line 6; and Claim 49, line 3, line 5: The terms "the gate stack" lack proper antecedent basis.

Claim Rejections - 35 USC § 102

2. Claims 41,45,46,50 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurimoto (5,306,655).

Kurimoto teaches a method (at Figs 13a-13h; col 13, line 21 through col 16) for forming a conductive gate of a metal oxide transistor comprising the steps of: forming a gate structure having a polysilicon gate electrode 5f formed on a gate oxide dielectric layer 2 formed on a semiconductor substrate (figs 13a; col 13, lines 30+); forming barrier sidewall nitride spacers 10 over sidewalls of the gate electrode and joining the dielectric oxide layer 2 by anisotropically etching a silicon nitride layer 10 (figs 13C-13D); and then oxidizing the substrate to channel oxidants through the gate dielectric layer 2 and underneath the spacers joined therewith and which is outwardly exposed laterally proximate the sidewall spacers, wherein only a portion of the gate electrode 5f, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 2 is oxidized (Fig 13f), while preventing oxidation of the upper parts of

side faces of the gate electrode 5f by the action of the barrier insulating nitride spacers 10 (col 13, lines 59-68), wherein as recited at column 18, lines 4-21, a third insulating film consisting of material which is not readily permeable to oxygen is formed over the gate electrode, wherein an intervening oxide layer is not formed between the gate electrode and the third insulating film.

3. Claims 41,45,46,50 are rejected under 35 U.S.C. 102(b) as being anticipated by Werhaar (5,015,598), with Hiroki et al (5,512,771) as an evidence, or alternative under 35 USC 103 (a).

Werhaar teaches a method (at Figs 1-5; col 4, line 30 through col 5) for forming a conductive gate of a metal oxide transistor comprising the steps of: forming a gate structure having a polysilicon gate electrode 12 formed on a gate oxide dielectric layer 11 formed on a semiconductor substrate 10 (col 4); forming barrier sidewall nitride spacers 20a laterally adjacent the sidewalls of the gate electrode 12 and joining the dielectric oxide layer 10 by anisotropically etching a silicon nitride layer 20 (col 4, lines 45-49; col 5, lines 10-52); and then oxidizing the substrate to channel oxidants through the gate dielectric layer 10 (col 5, lines 47-52) and underneath the spacers joined therewith and which is outwardly exposed laterally proximate the sidewall spacers, wherein only a portion of the gate electrode 12, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10 is oxidized (Fig 5), while preventing oxidation of the upper parts of side faces of the gate electrode 12 by the action of the barrier insulating nitride spacers 10. Since Werhaar discloses forming the silicon nitride spacers 20a having a thickness between 15 and 50 nm and preferably close to 30 nm (col 4, lines 63-68) adjacent to the gate electrode 12; and since oxidizing at 900°C for a duration of 15 to 30 minutes in oxygen to form a silicon oxide layer 24 (fig 5) having a thickness of the order of 10 to 15 nm (100 to 150 Angstroms), only a portion only a portion of the gate electrode 12, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10 is inherently oxidized and creating a "smiling gate" (can be seen by enlarging the gate electrode). It is the fact that the present specification discloses (at page 7, lines 14-19) that only portion of the gate electrode is oxidized in a time period for growing "an oxide layer over a separate semiconductor substrate to a thickness of a round 80 Angstroms". Herein, since Verhaar grows a silicon oxide layer 24 having a thicker thickness of 100 to 150 Angstroms, only a portion of the gate electrode, laterally adjacent the sidewall spacers and at the interface with the gate dielectric oxide layer 10,

is inherently oxidized ("smiling gate"). Consequently, the burden shifted to applicant to demonstrate and prove that this apparent inherence does not in fact exist, In re King, 801 F.2d 1324, 1327, 231 USPQ 136, 138-139 (Fed. Cir. 1986).

Hiroki et al (5,512,771) is cited to evidently teach that the oxide layer 6' formed under the silicon nitride spacer 7 allows oxidizing substance to transmit therethrough to oxidize a portion of the gate electrode (col 12, lines 10-21; figs 6A-6B). Moreover, it would have been obvious to ordinary skill in the art to create a "smiling gate" as taught by Hiroki et al, because of the desirability to have smaller gate-to-drain capacitance and thus to improve the speed of the circuit operation (col 8, lines 45-67; fig 2).

Claim Rejections - 35 USC § 103

4. Claims 43,47 are rejected under 35 U.S.C. § 103(a) as being unpatentable over either Kurimoto (5,306,655) or Verhaar/Hiroki et al, in view of Pintchovski et al (5,126,283).

Kurimoto or Verhaar already teaches a method for forming a conductive gate of a metal oxide transistor as applied above to claims 41,45,46,50, but lack to form a gate electrode having a polysilicon, a conductive reaction barrier layer, and an overlying metal (re claims 43,47).

However, Pintchovski et al teach (at figs 3a-3c; col 5, line 60 through col 6, line 45) to alternatively form a gate electrode having a polysilicon layer 38, a conductive reaction barrier layer 40, and an overlying metal 42.

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to form a multi-layered transistor gate electrode as taught by Pintchovski et al because of the desirability to fabricate high speed devices due to high conductivity of the gate electrode, wherein the conductive reaction barrier layer also acts as a diffusion barrier.

5. Claims 44,48,49,51,52 are rejected under 35 U.S.C. § 103(a) as being unpatentable over either Kurimoto (5,306,655) or Verhaar/Hiroki et al (5015598 & 5512771), in view of Pintchovski et al (5,126,283), as applied to claims 41,43,45-47,50 above, and further of Brigham et al (5,714,413) and Kumagai et al (5,430,313).

Kurimoto or Verhaar already teaches to form single sidewall barrier spacers 10 over sidewalls of the gate (Fig 13), which teaching is similar to a first embodiment of the present invention as shown in figure 3, in which single sidewall barrier spacers 34 are used.

The further main difference between the references applied above and the instant claim(s) is as follows: instead of using single sidewall spacers (first embodiment, fig 3 of present application), the present application, in a second embodiment (fig 5) and a third embodiment (fig 7), alternatively teaches to use double sidewall spacers by etching first and second material layers.

However, Brigham et al teach (at figs 2b-2c,3c; col 6, line 60 through col 7, line 6; cols 4-6) to form double sidewall spacers by depositing a second material layer on a first material layer and anisotropically etching the first and second layers to form double sidewall spacers, wherein Brigham expressly teaches "three or more layers of dielectric...are implemented to form a multi-layered spacer structures" (col 6, lines 1-6), and wherein silicon nitride is disclosed. Kumagai et al teach (at figs 4B-4D; col 3, line 65 through col 4, line 15) to form single sidewall nitride spacers 16 on sidewalls of a gate 14, and alternatively, forming double sidewall nitride spacers including first sidewall nitride spacers 16 and second sidewall nitride spacers 30 by anisotropically etching a deposited first material barrier layer and then anisotropically etching a second deposited material barrier layer (figs 7A-7D; col 5, line 45 through col 6).

The subject matter would have been obvious to one of ordinary skill in the art at the time the invention was made to alternatively form single sidewall nitride spacers or double sidewall spacers on the sidewalls of the gate as combinatively taught by Brigham, Kumagai, Kurimoto, and Verhaar. This is because of the desirability to substitute and alternatively use the single sidewall nitride spacers or the double sidewall spacers as a barrier mask during oxidation to form an oxide film. This is also because of the desirability to employ the double sidewall spacers as a mask during implantation to form source and drain regions at a predetermined distance from the gate electrode.

Response to Arguments

6. Applicant's arguments filed Sep 28, 2000 have been fully considered but they are not persuasive, and to are also moot in view of the new ground(s) of rejection.

** Regarding 102 rejection using Kurimoto: Applicant mainly remarks about claims 41, 45, 50, and 52 (at remark pages 5-8) that "Kurimoto oxidizes the gate structure prior to forming any sidewall spacers..." (remark page 6, lines 11-17), and "...such a structure having the aforementioned intervening oxide layer..." (remark page 6, lines 19-21). It is noted and

found unconvincing. Although figures 13a-13h, col 13, lines 37-52 of Kurimoto show an intervening oxide layer, Kurimoto also recited a method (at column 18, lines 4-21) that, after the step of forming a gate electrode by anisotropically etching (col 18, lines 4-10), third insulating spacers consisting of material which is not readily permeable to oxygen (e.g. silicon nitride spacers 10) are formed only upon side faces of the gate electrode 5f, wherein an intervening oxide layer is not therefore formed between the gate electrode and the third insulating film.

** Regarding 103 rejections: Applicant mainly remarks that "Applicant has shown, above, that Kurimoto does not teach...forming a nitride or oxidation resistant spacer adjacent the gate structure...the rejection is in error...". However, as shown above by the examiner that Kurimoto also discloses to form a nitride or oxidation resistant spacer adjacent the gate structure since an intervening oxide layer is not needed between the gate electrode and the third insulating oxidation resistant spacers. Accordingly, the 103 rejections are maintained.

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Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

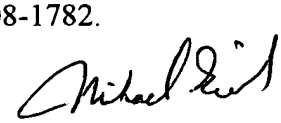
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Whitehead Jr Carl can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Oasc



Michael Trinh
Primary Examiner